REMARKS

Claims 1-12 are pending in the present application. Claim 1 is amended. The amendment to claim 1 is supported in the specification as filed at page 6, lines 17-18. No new matter is added by the claim amendment. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Claims 1-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Laparra *et al.* (U.S. 6,319,796 - hereinafter "Laparra") in view of Park *et al.* (U.S. 6,326,282 - hereinafter "Park"). It is requested that this rejection be reconsidered and removed in view of the foregoing amendment and the following remarks.

The present invention as claimed in amended independent claim 1 is directed to method for providing trench isolation in a semiconductor device. An etching mask pattern is formed on a semiconductor substrate to expose a predetermined region of the semiconductor substrate. The exposed semiconductor substrate is then etched, using the etching mask pattern as an etching mask, to form a trench. An insulating layer is formed over the trench and nearby regions, the insulating layer filling the trench. A high-temperature oxide (HTO) layer is provided on the insulating layer, the HTO layer being formed at a temperature of 700C to 800C. The HTO layer and the insulating layer down are planarly etched to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench. The exposed etching mask pattern is then removed.

In this manner, the method of the present invention as claimed in amended claim 1 provides for densification of the insulating layer (see for example, reference 23 of FIG. 1F), by virtue of formation of the HTO layer (reference 24 of FIG. 1F) at a temperature of 700C - 800C.

Accordingly, there is no need to perform an additional annealing process, which otherwise could lead to a number of process limitations, as specified in the present application as filed at page 2, lines 2 - 23.

With regard to the Park reference, Park teaches that a PE-oxide layer (or PE-TEOS layer) 118 is formed on the underlying USG layer 116 (see FIG. 2D). However, either "plasma-enhanced", or PE, process utilized in Park, namely the PE-oxide or PE-TEOS process (PE refers to "plasma-enhanced"), would be performed at a relatively low temperature, for example 400 C or lower, as is well known in the art. The application of the PE-oxide or PE-TEOS layer is for the mere purpose of relieving stress in the underlying USG layer (Park, column 4, lines 63-65), and, due to the low-temperature application, does not result in densification of the underlying USG layer. As a result, the Park process requires a subsequent annealing process in order to densify the USG layer (Park, column 4, line 66 - column 5, line 5).

With regard to the Laparra reference, Laparra teaches application of coating 40B as a "continued application of silica-based material", for example an "HDP deposition" (Laparra, column 4, lines 4- 21), or, alternatively, may comprise an low-pressure chemical vapor deposition (LPCVD) of a TEOS-based dielectric (Laparra, column 4, lines 51-56).

In view of the above, it is submitted that neither Park nor Laparra, alone or in combination, teaches or suggests the present invention as claimed in amended claim 1. Specifically, neither reference teaches or suggests "providing a high-temperature oxide (HTO) layer on the insulating layer, the HTO layer being formed at a temperature of 700C - 800C ".

Accordingly, reconsideration of the rejection and allowance of claim 1 are respectfully requested. With regard to the various dependent claims 2 and 4-12, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims:

Claim 1 is amended above as follows:

1. (Amended) A trench isolation method for forming a semiconductor device comprising:

forming an etching mask pattern on a semiconductor substrate to expose a predetermined region of the semiconductor substrate;

etching the exposed semiconductor substrate, using the etching mask pattern as an etching mask, to form a trench;

forming an insulating layer over the trench and nearby regions, the insulating layer filling the trench;

providing a [material] high-temperature oxide (HTO) layer on the insulating layer, the [material] HTO layer being formed at a temperature of 700C - 800C [of 500°C and higher];

planarly etching the [material] HTO layer and the insulating layer down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench; and

removing the exposed etching mask pattern.